A DC-12 GHz Monolithic GaAsFET Distributed Amplifier

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Abstract—**A monolithic balanced traveling-wave amplifier stage using GaAs MESFET's is demonstrated. This amplifier achieves 7–9-dB gain with about 40-ps risetime and a −3-dB bandwidth of 12 GHz, on a 0.91×0.97-mm die. Its gain versus frequency is very flat, and $|S_{11}|$, $|S_{12}|$, and $|S_{22}|$ are less than 0.2 from 0–18 GHz. *S*-parameter uniformity and yield data are measured on-wafer with a special hybrid wafer probe.**

I. Introduction

SINCE 1937, the distributed or traveling-wave amplifier topology [1] has found many applications in broadband amplifiers. Historically, distributed amplifiers were first realized by using thermionic devices for active elements. Design considerations for various transmission-line sections, tapered plate lines, paired grid or plate connections, grid loading, line losses, staggered phase velocities, transient response, noise figure, optimal usage of active elements, and other topics have been studied [2], [3]. More recently, distributed amplifiers have been realized by using silicon bipolar transistors [4]–[6], MOSFET's [7], and MESFET's [8], as well as GaAs MESFET's [9]. The recent availability of high-quality semi-insulating GaAs and sufficient GaAs processing maturity make distributed amplifier stages using GaAs MESFET's integrated with all the required passive components an attractive circuit approach for ultra-broad-band amplification. In this paper, we discuss some design considerations for GaAs distributed amplifiers, our choice of a design for pulse amplification, and the GaAs processing used. This is followed by frequency- and time-domain measurement results and an appendix describing on-wafer probing techniques for frequencies through 18 GHz.

II. Amplifier Design

The low-frequency voltage gain of a distributed amplifier (as in Fig. 1, but assuming lossless lines and $R_g \gg Z_0$) is $Ng_mZ_0/2$, where N is the number of sections or FET's, g_m is the transconductance of each FET, and Z_0 is the characteristic impedance of the output transmission line. The cutoff frequency of this simple LC line is $(\pi\sqrt{LC})^{-1}$, where L is the inductance of each coil, and C is C_{gs} for the gate line, or $C_{ds}+C_p$ for the drain line. Monolithic integration of the FET's and inductors allows delays per section of 10 ps or less, implying cutoff frequencies greater than 30 GHz. However, other GaAs MESFET parasitics limit the distributed amplifier's gain above 10 GHz to less than the low-frequency gain. The input line divides the input power and the output line combines the power from each FET, while each also performs some sort of impedance matching to the FET's. Thus, the gain of a distributed amplifier stage is limited to the maximum available gain (MAG) of an individual device in the amplifier. The traveling-wave topology simply provides more options in the design of the matching networks than in amplifiers with single active devices.

The measured and modeled *S*-parameters of the 0.7×300-μm FET's used in the amplifiers are shown in Fig. 2. These measurements were done with the wafer probe described in the Appendix, and the equivalent-circuit calcula-

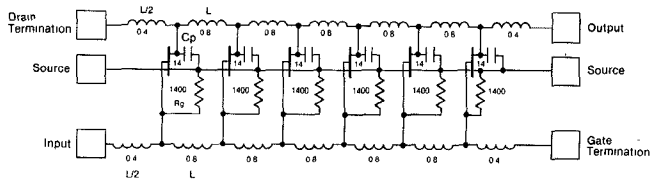

Fig. 1. Schematic of the six-section single-ended GaAs FET distributed amplifier. The squares depict the bond pads used; on most amplifiers, the gate and drain terminations were supplied off-chip, i.e., mounted on the RF probes or on the BeO substrate. Each FET is modeled as in Fig. 2. The ten-section amplifier used the same topology but proportionally smaller FET's, capacitors, and inductors, and larger R_g's.

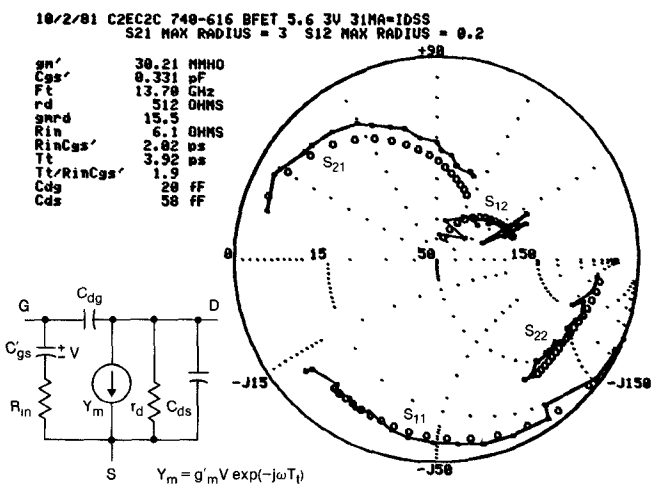

Fig. 2. Measured 2–18-GHz *S*-parameters of a typical 0.7×300-μm FET, using the microwave wafer probe. The circles are *S*-parameters of the simplified equivalent circuit calculated from the measured parameters.

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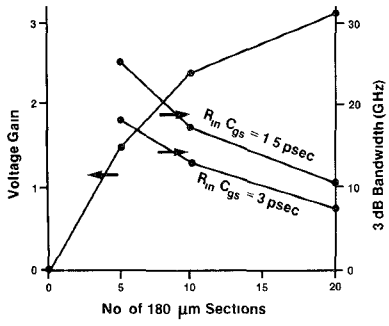


Fig. 3. Calculated gain and bandwidths of distributed amplifiers with different numbers of sections. Each section uses a 0.7×180-μm FET, and typical practical parasitics are included in these simulations.

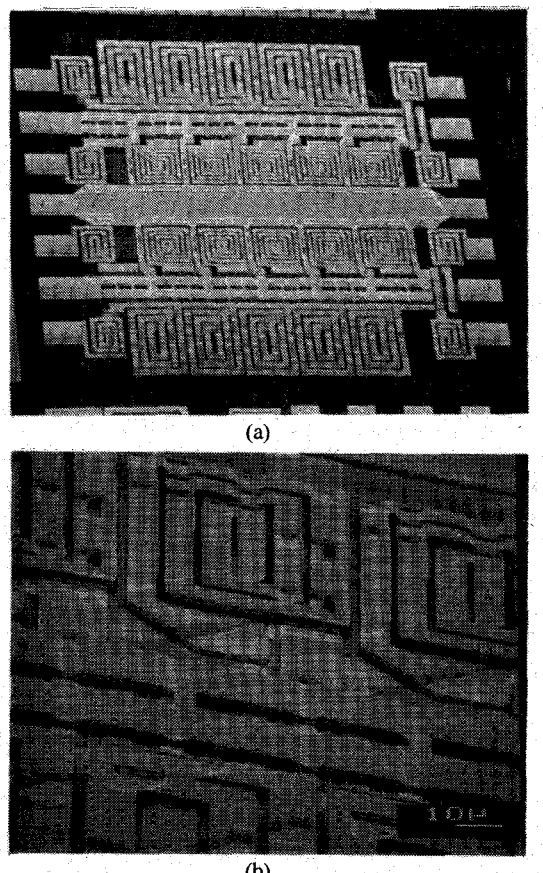
tion routine was written into the network analyzer software. This simplified equivalent circuit absorbs some of the physical parasitics of the device into other elements, yet adequately describes the FET's up to 18 GHz [10]. The maximum stable gain of this device is about 18 dB at 4 GHz, decreasing to about 10 dB at 18 GHz. The feedback capacitance C_{dg} is low enough in GaAs MESFET's to not cause gain variations with frequency in the distributed amplifier.

The main FET parasitic which decreases the high-frequency gain is R_{in}, the resistance in series with C_{gs}. As R_{in} decreases, the amplifier bandwidth increases until it is limited by the cutoff-frequency of the transmission lines (as R_{in} decreases, the MAG of the FET increases). The R_{in} of the FET's shown in Fig. 2 causes a smooth gain rolloff with frequency which is suitable and, in fact, desired for good transient response. The addition of series resistance on plate or grid lines has been used to improve the transient response of distributed amplifiers using vacuum tubes [11]. As the input signal travels down the gate line, each FET sees less and less high-frequency energy, since the R_{in} of the previous FET's dissipated more power at high frequencies than at low frequencies. Thus, increasing the gain of the amplifier by adding sections decreases the amplifier's bandwidth because the signal on the gate line contains less high-frequency power the further the signal propagates down the gate line. To study the effects of all the possible parasitics, SPICE2 simulations of the full amplifier were performed iteratively while varying the circuit elements. Fig. 3 shows SPICE2 calculations of the gain and −3-dB bandwidth versus number of sections for an amplifier stage using 0.7×180-μm FET's and practical parasitics. From this study, a total FET width of 1800 μm was chosen, for a total g_m of about 180 mS.

50-Ω input and output impedances were used, and equal-delay low-pass sections with uncoupled inductors and equal input and output phase velocities were chosen. This design was chosen partly for its simplicity; it should be noted that many other design possibilities exist. For example, sections having nonequal FET widths and inductors, and/or tapered drain lines [3] may be very useful. Two amplifiers were realized with different delays per section but with the same total FET width: one used six sections of 0.7×300-μm FET's, and the other used ten sections of 0.7×180-μm FET's. The cutoff frequencies are about 20 and 35 GHz, respectively. The layout of the six-section amplifier allowed spiral coils with slightly higher Q than those for the ten-section amplifier. The ten-section amplifier was designed to provide increased bandwidth as processing techniques which reduce $R_{in}C_{gs}$ are developed. The main difference between the measured performance of the two is that, as expected, the cutoff frequency of the transmission lines in the six-section amplifier decreases the gain rapidly above 16 GHz. The amplifiers were realized in mirror-image balanced pairs, with a virtual ground between the two sides. Balanced amplification eliminates the need for very low inductance source connections to ground, and greatly simplifies the dc design.

To effectively use the GaAs area and minimize the inductance between the sources in the two sides of the balanced amplifier, lumped spiral inductors were chosen over microstriplines for the transmission lines. The inductances were calculated by using a simple program that adds up the self- and mutual-inductances of straight-line segments of conductors in arbitrary positions [12], [13]. The inductance reduction due to the presence of a ground plane is analyzed by the method of current images. Assuming the ground plane is a perfect conductor, the ground plane causes the same effect as that of an identical spiral inductor two substrate thicknesses below the real inductor, having equal current but flowing in the opposite direction. The coil inductances calculated in this manner are typically within 40 pH of the measured values. The flexibility of this program allows investigation of complex shapes and the mutual inductance between coils. The 0.8-nH coils on the six-section amplifier are placed adjacent to each other, yet have less than 20-pH mutual inductance.

The ohmic losses in the spiral inductors is significant. Each inductor in the six-section amplifier has a dc resistance of about 2 Ω. This resistance could be reduced by making the spiral dimensions much larger, but doing so causes other layout problems and a lower self-resonance frequency. The inductors used in these amplifiers are free of resonances up to 18 GHz (Fig. 8). The loss due to the inductors directly affects the noise figure and maximum output power from the amplifier. Since lowest noise figure and maximum output power are not stringent requirements in this amplifier's application, very small inductors were used to minimize chip area. To improve the return loss and time domain distortion caused by the inductor series resistance, a small conductance (R_g in Fig. 1) was intentionally added to the gate transmission line. This conductance makes the gate line's characteristic impedance nearly independent of frequency when $R_g = Z_0^2/R_L$, where R_L is the series resistance of the inductors (if R_L is independent of frequency). However, R_L increases with $\sqrt{f}$ at high frequencies due to skin effect in the 2-μm-thick air-bridges. This increasing resistance with frequency causes the addition of R_g to be only partially effective in improving the pulse distortion, and causes an additional slow rolloff of gain with frequency. In contrast to the gate line, the drain terminal of the FET presents parallel resistance (r_d) and



(a)

(b)

Fig. 4. Scanning electron micrographs of the six-section amplifier. The whole balanced amplifier is shown in (a) with mirror-image halves. The higher magnification view in (b) shows the gate coils at the bottom, FET's in the center under the two source air-bridges, and drain coils at the top.

capacitance (C_{ds}) to the drain line. The drain resistance r_d has the same effect on the drain line that R_g has on the gate line.

The electrical design must be iterated with the layout of such an amplifier to ensure that significant parasitics such as inductor series resistance are included in the models. In addition to the intentional elements shown in Fig. 1, the inductor series resistance and mutual inductance and capacitance, source inductances, and a variety of FET parameters were included in the computer models. SEM's of the six-section amplifier are shown in Fig. 4. The layout is very compact and allows RF probing of inputs, outputs, and terminations (see Appendix). Air-bridges are used extensively for interconnects and for elevating most of the spiral inductors to reduce interturn capacitance.

The processing was generally conventional. Active and $N+$ layers were formed by implanting silicon through 100 nm of SiO_2 into undoped semi-insulating substrates; photoresist was used as an implant mask. The active layer implant was $6\times10^{12}/cm^2 Si^+$ at 130 keV, resulting in a pinchoff voltage of -2.3 V. Gate, ohmic, and resistor metal lithography was by optical contact printing of positive resist, followed by etching of a Si_3N_4 passivation layer, metal evaporation, and aided liftoff. Ohmic contacts were alloyed AuGe–Ni, and the gate metal was Ti/Pd/Au. The gate length was 0.7 μm. The resistors were 50-Ω/sq NiCr, and the capacitors were formed between the gate metal and air-bridge metal by using 100 nm of Si_3N_4 as a dielectric. A total of three layers of Si_3N_4 were used. Air-bridges were formed by patterning a 2-μm layer of photoresist with the via pattern, depositing a Ti/Au layer, applying a second layer of photoresist and patterning with the air-bridge pattern, and plating gold to a thickness of 2 μm. The photoresist layers and the Ti/Au layer were then removed. The coils were made of air-bridge metal elevated above the Si_3N_4/GaAs surface with periodic contact to the surface for support. The air-bridges proved to be surprisingly rugged.

III. Measurements

All of the FET and inductor modeling data and most of the amplifier data discussed here were taken with the microwave wafer probes discussed in the Appendix. The basic test is the measurement of two-port S-parameters from 2–18 GHz for one-half of a balanced amplifier (i.e., a single-ended amplifier), with a corrected network analyzer calibrated at the probe tips. Fig. 5 shows the magnitude of the gain of a six-section amplifier plotted versus frequency for seven different gate bias voltages. Decreasing the gate bias drops the gain due to the decreasing g_m of the FET's in the amplifier. As the FET's are pinched off, $|S_{21}|$ approaches $|S_{12}|$, resulting in a 20-dB gain-control range below 10 GHz. $|S_{12}|$, $|S_{11}|$, and $|S_{22}|$ remain less than 0.2 for all these gate bias conditions over 2–18 GHz. This insensitivity to bias shows how insensitive the amplifier is to FET parameter variations, because C_{gs} of one of these 0.7×300-μm FET's varies from 0.35 pF to 0.11 pF over this bias range.

The uniformity and yield of amplifiers was measured using the microwave wafer probe. Fig. 6 shows the S-parameter magnitudes of 17 out of 20 ten-section amplifiers in one column spanning a two-inch wafer. Below 10 GHz, the gain variations from amplifier to amplifier are ±0.5 dB, and all the other S-parameter magnitudes are less than 0.18. More extensive mapping of wafers reveals a typical yield of 70 percent on single-ended amplifiers.

The frequency-domain corrected S_{21} measurements over 0–18 GHz were inverse Fourier transformed (IFT) with raised-cosine windowing [14] to determine the transient response. The IFT-measured responses are identical to the sampling-measured response shown in Fig. 7, except that the inverse Fourier transformed data showed a good fast transition up to about 90 percent of the final output value, instead of the 85 percent measured on the packaged balanced amplifier with the sampler. The risetime measurement is significantly degraded by the rise time of the system (about 35 ps for transformed data), thus the amplifier calculated risetime is a relatively sensitive function of the system risetime and of the total measured risetime. The amplifier risetime measured in several different ways averages about 40 ps.

Packaged single-stage DC-12 GHz balanced amplifiers

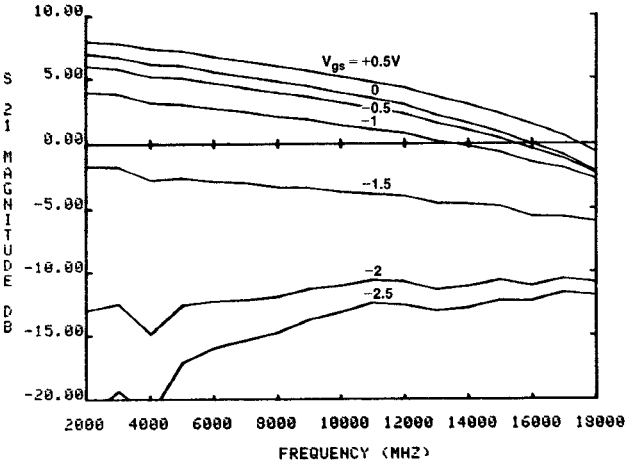


Fig. 5. Magnitudes of $|S_{21}|$ of a six-section amplifier versus frequency for gate-source biases of 0.5, 0, −0.5 −1, −1.5, −2, and −2.5 V.

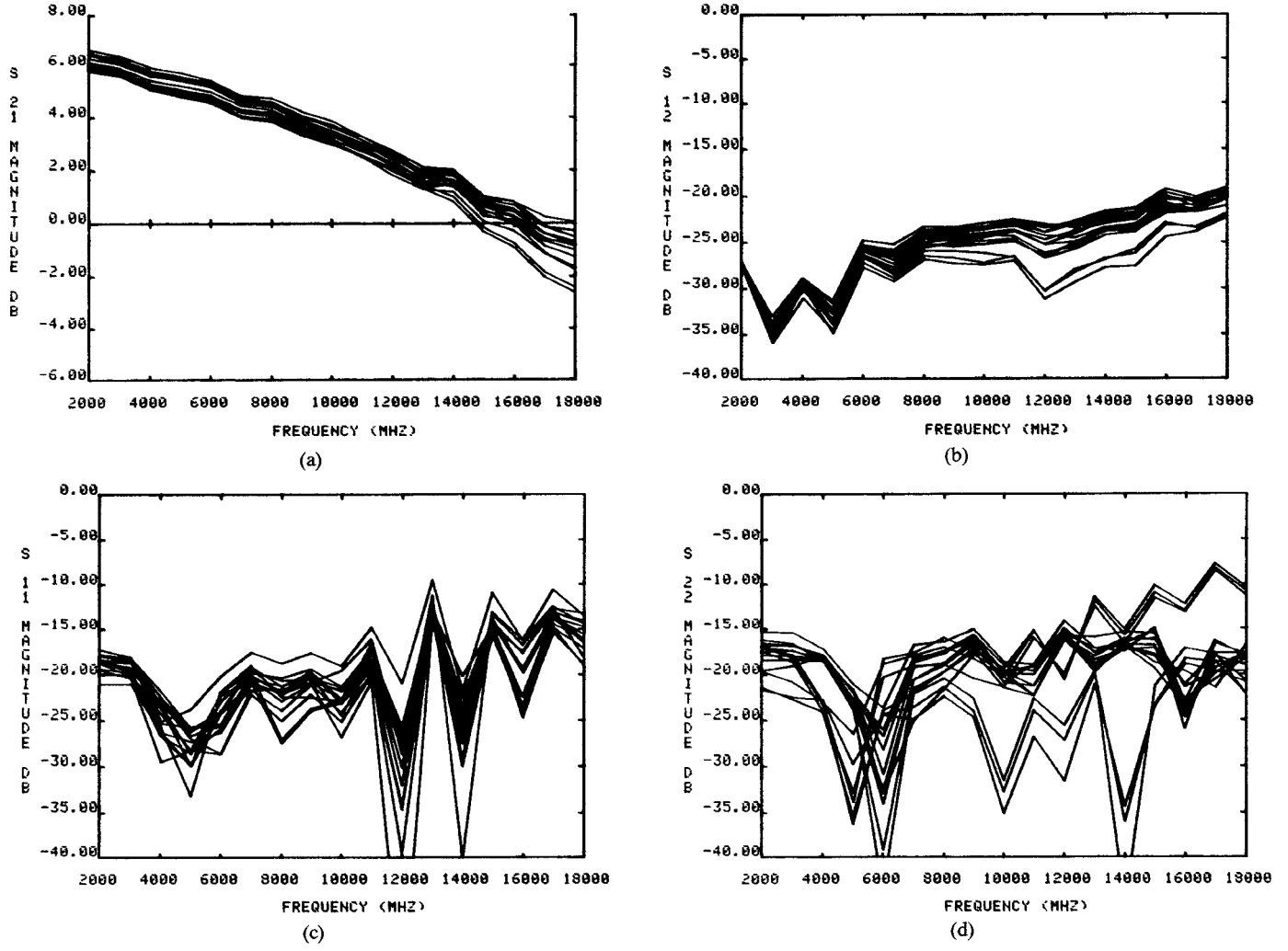


Fig. 6. S-parameters of 17 ten-section amplifiers measured on-wafer, showing the variations from die to die. (a) shows $|S_{21}|$, (b) shows $|S_{11}|$, (c) shows $|S_{12}|$, and (d) shows $|S_{22}|$. $V_{ds} = 5$ V and $V_{gs} = 0$ V for each of these tests.

were realized on 13-mil BeO substrates by using either the six-section or ten-section amplifiers lapped to 100-μm thick. 50-Ω microstriplines and NiCr terminations on the BeO substrate were bonded to the amplifier transmission lines just before the end half-coils. In this fashion, the bond wires's excess inductance is used as part of the amplifier

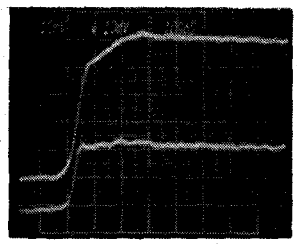


Fig. 7. Balanced amplifier response (top) to a balanced time-domain step generator (bottom). The vertical scale factor is 100 mV/div for both traces. The absolute time relation between the input and output is actually a 90-ps delay.

transmission line. No tuning elements or bypass capacitors were used on the hybrid. The amplifier response to a balanced 25-ps tunnel-diode step generator was measured with balanced 20-ps samplers (Tektronix type S-6) and is shown in Fig. 7. The output step shows a fast rise up to about 85 percent of the final value. The remaining 200-ps rise ("dribble-up") is partially due to the input pulse shape, but is mainly due to skin effect in the amplifier transmission-line inductors. This shape is typical of pulse distortion from any type of transmission line having significant skin-effect losses [15], and can be equalized in various ways. This measurement is done with 200-mV pulses, but it appears that output pulses up to 6-V amplitude will have similar shapes.

The amplifier noise figure was measured from 2–4 GHz, although neither the FET structure nor the amplifier was designed for low noise. At 2 GHz, the noise figure of the single-ended six-section amplifier with a 50-Ω source impedance was typically 5.7 dB, increasing to 6.4 dB at 4 GHz. The ten-section amplifier had noise figures averaging 0.34 dB higher at these frequencies. 150 amplifiers were measured using the microwave wafer probe; the standard deviation of the noise figure for either amplifier type was 0.24 dB. The probe's noise contribution was determined by de-embedding the probe with the same calibration standards as were used for the *S*-parameter measurements [16], [17].

Clearly, such an amplifier has many potential applications in pulse or frequency-domain generation and measurement instrumentation. The transient response requirement of a pulse amplifier necessitates class A operation and 50-Ω input and output impedances from dc up to the highest frequency passed by the amplifier. Thus, a large part of the dc input power to the stage is dissipated in the drain-load resistors; one balanced amplifier stage including load resistors dissipates 3–10 W, depending on the drain bias. For applications where dc response is not necessary, elimination of the dc current in the terminations would reduce the power dissipation of the stage to approximately that of the FET's alone. The maximum output power or distortion for frequency-domain signals was not measured.

IV. Conclusions

The distributed amplifier topology is well-suited for GaAs MMIC designs. Its merits include ultra-broad-band gain with good flatness, very low reflections on both the input and output, reverse transmission similar to that of the FET's, a low sensitivity to device parameters, high stability factor, and good transient response. For some applications, the inherent redundancy of active devices may be useful for enhanced reliability. With a MMIC realization, the amplifier's bandwidth is limited by high-frequency losses in the gate line due to the gate charging resistance of the FET's, and by skin effect in the inductors.

By using a segment-by-segment inductance calculation, it was found that inductors can usually be packed adjacent to each other without significant coupling. This amplifier was not intended for a low-noise or high-power application, so significant loss in the transmission lines was accepted to keep the inductor area low. High yields and uniformities were achieved. With yields of 70 percent, gain spreads of ±0.5 dB, small size, and a layout allowing RF probing, this amplifier is potentially very cost effective.

Finally, the microwave wafer probe was found to be extremely useful for gathering modeling and statistical data accurately, quickly, and nondestructively before packaging. RF probing constraints are now included in our design rules for all circuits. Besides in-houses uses, an RF probing standard as an interface for purchased devices in chip form would save much time and would enhance measurement accuracies for both suppliers and users. Further development can yield standard specifications for probes and on-wafer calibration standards.

Appendix

Microwave Wafer Probe

The obvious need for accurate probing methods for microwave components has existed for many years. Progress in this area has been hampered by the relatively small dimensions of the components, the radiation impedance of short probe tips, and the need to make backside contact to some types of devices. Previous probe work has achieved usable device data up to 4 GHz [18] by using convergent 50-Ω microstriplines with short wire tips contacting the bond pads of the device under test (DUT) through a hole in the probe substrate. This type of probe was studied [19] by building a probe with wire probe tips extending about 35 mils beyond the microstrip substrate; the self-inductance of each wire tip was about 0.4 nH. A corrected network analyzer can remove the effect of this much series inductance from *S*-parameter measurements except when the inductance is in the common lead of a multiport device. Moreover, it was found that even measurements on one-ports were not repeatable above about 4 GHz and that this was due to surprisingly large changes in the radiation impedances of the wire tips as the wafer chuck or nearby conductors were moved.

Therefore, probes were designed to bring the 50-Ω environment closer to the DUT with minimal ground inductance between the probe transmission lines and the DUT. The first of these probes [19] used a 50-Ω microstrip line where the width at the coaxial connector was 10 mils but stepped to a 27-μm width about 5 mm from the probe tip

(with a corresponding step in the distance to the ground plane to maintain the characteristic impedance). By tilting the microstrip board, the transmission line and ground plane at the tip can be brought into direct contact with the device's bond pads (typically on 100-μm centers). The only intervening structure, in contrast to wire probe tips, was a gold ball 1 mil in diameter that provided a large contact area and tolerated slight nonplanarities between the probe tip and the device pads. Devices with as many as ten signals plus ground contacts have been tested in this fashion. The critical dimensions of these structures are all lithographically defined and therefore are very repeatable and relatively easy to mass produce. This probe was shown to have excellent repeatability in corrected network analyzer measurements of one-ports and two-ports.

More recently, it was found that coplanar waveguide (CPW) [20] tapered from the coaxial transition to the probe tip could perform the function of shrinking the 50-Ω environment to dimensions commensurate with the bond pads. Grounding straps to equalize the ground potentials on either side of the signal lines are necessary, and gold balls are used to contact the device pads, as above. These probes are very simple to fabricate, requiring only one patterned metallization on the substrate. Measurements made with these CPW probes are nearly as repeatable as those made with the stepped-microstrip probes.

One very beneficial usage of these probes has been for the measurement of small-signal S-parameters with a corrected network analyzer calibrated at the probe tip(s). A series of on-wafer calibration standards were simultaneously developed. Using these standards, losses and reflections from the probe lines and transitions to coax can be canceled out in addition to those errors resulting from the cables and the network analyzer. Thus, all of these probe measurements are of the devices looking into their bond pads without any bond wires. When the probe is used in this fashion, the measurement accuracy is limited by the repeatability of the probe's parameters rather than by its loss or return loss. (One line of a probe typically has 10-dB return loss through 18 GHz). The repeatability of the probe contacts is much better than that of typical SMA connectors, and bonding repeatability problems are eliminated.

Fig. 8 shows one-port measurements of some of the impedance standards after calibrating the system with a short, a 50-Ω termination, and an open circuit (small capacitance). Since the impedance standards are much smaller than a wavelength, their equivalent circuits are simple lumped elements that can be measured at low frequency or that can be predicted from their dimensions. The short standard used was simply a large area of metallization at least 10-mils square. The standard bond pads used are 50-μm wide on 100-μm centers. A 50$\times$150-μm rectangle (just large enough to short the signal ball to the ground ball on the probe) theoretically and experimentally has about 30 pH of inductance. The 50-Ω resistor used is a 40-μm square NiCr resistor deposited on GaAs. Its resistance can be measured at dc, and its series inductance is about 30 pH. For an open circuit, the probes are placed either on unconnected bond pads or on an unused area of semi-insulating GaAs. The stray capacitance was empirically determined to be about 3 fF by ensuring that the corrected reflection coefficient magnitudes of high-Q coils and capacitors were less than one. As can be seen in Fig. 8, the resulting measurements are extremely tightly grouped and clearly demonstrate the lumped nature of these elements.

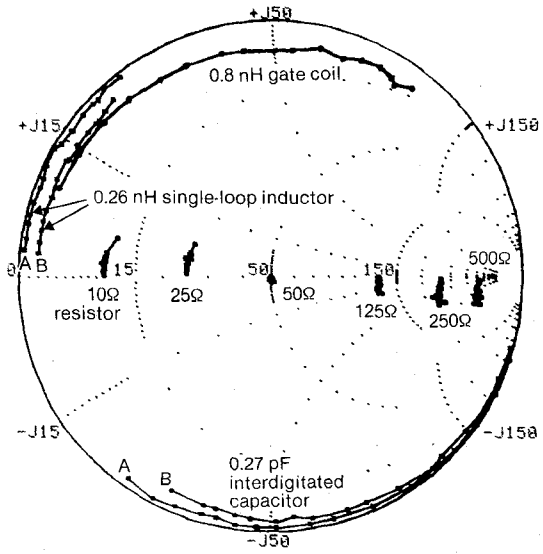


Fig. 8. Corrected 2–18 GHz one-port measurements of various on-wafer impedance standards and a single 0.8-nH spiral inductor like those used in the six-section amplifier. All the resistors are made with 50-Ω/sq NiCr. The 50-Ω resistor is used for the zero-reflection standard without compensating for its inductance. The measurements labeled "A" are of elements realized in 2-μm thick Au; those labeled "B" are of the same elements realized in 0.5-μm thick Au.

Two-port corrected S-parameter measurements use the above calibration for each port, plus through connection and isolation calibration standards. The through standard simply connects the two ground contacts together and the two signal contacts together. As yet, the best isolation standard found connects the two ground contacts together but leaves the signal contacts open. The standard twelve-element ("full") error-correction model [21] for two-port network analyzers ignores several possible isolation error terms. The result is that when calibrating through a fixture that has significant crosstalk, the isolation calibration is valid only when the S_{11} and S_{22} of the DUT are equal to the S_{11} and S_{22} of the isolation standard used. The crosstalk between two-probe substrates is negligible when the probes are in air but is on the order of -30 dB when they are contacting a device. High-attenuation transmission measurements, e.g., S_{12} of FET's and amplifiers, are the least accurate due to this incomplete error modeling.

Clearly the devices to be probed must conform to pad configurations for which the probes are designed (or vice versa). The limitations are that the pads to be probed must be in rows accessible to the probes, and that each line of pads must have at least one ground or common pad (as in Fig. 4). For simplicity, standard pad spacings and only two parallel rows of pads (one on either side of a device) are

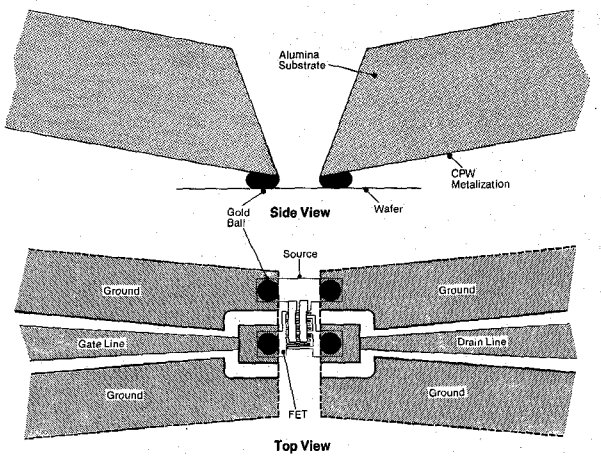


Fig. 9. Top and side views of two CPW probes contacting a discrete FET.

used whenever possible. Fig. 9 shows a typical FET and CPW probes being used to measure it. The two-probe boards are mounted on separate three-axis positioners, so the relative position of the two rows to be contacted can easily be changed, although the ground/signal designation is fixed. 50-Ω terminations have been mounted on the probe tips for multiport *S*-parameter measurements, and other passive or active elements can be printed or mounted on the tips for further testing capabilities.

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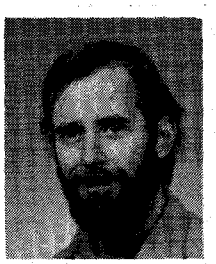

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